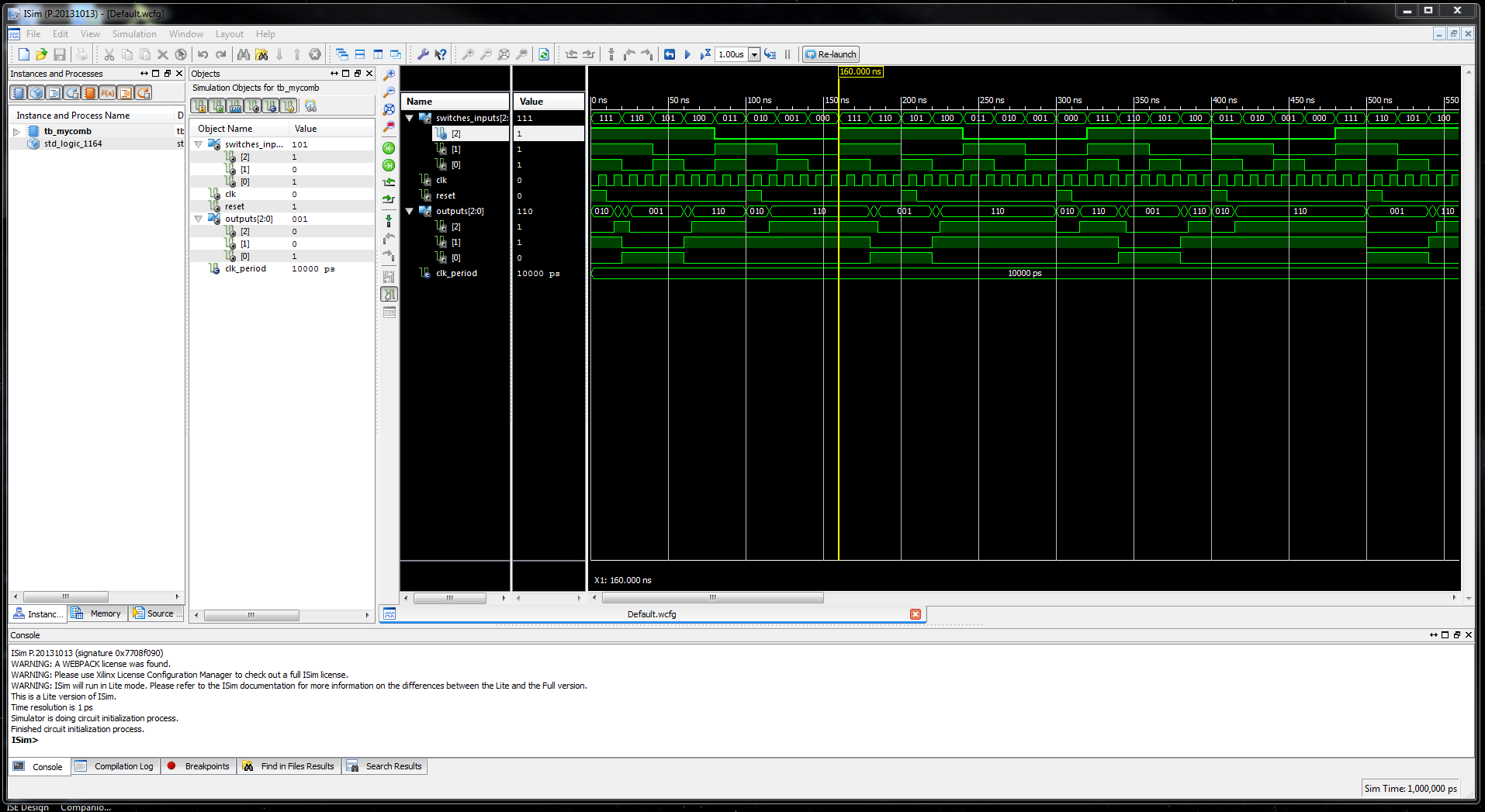
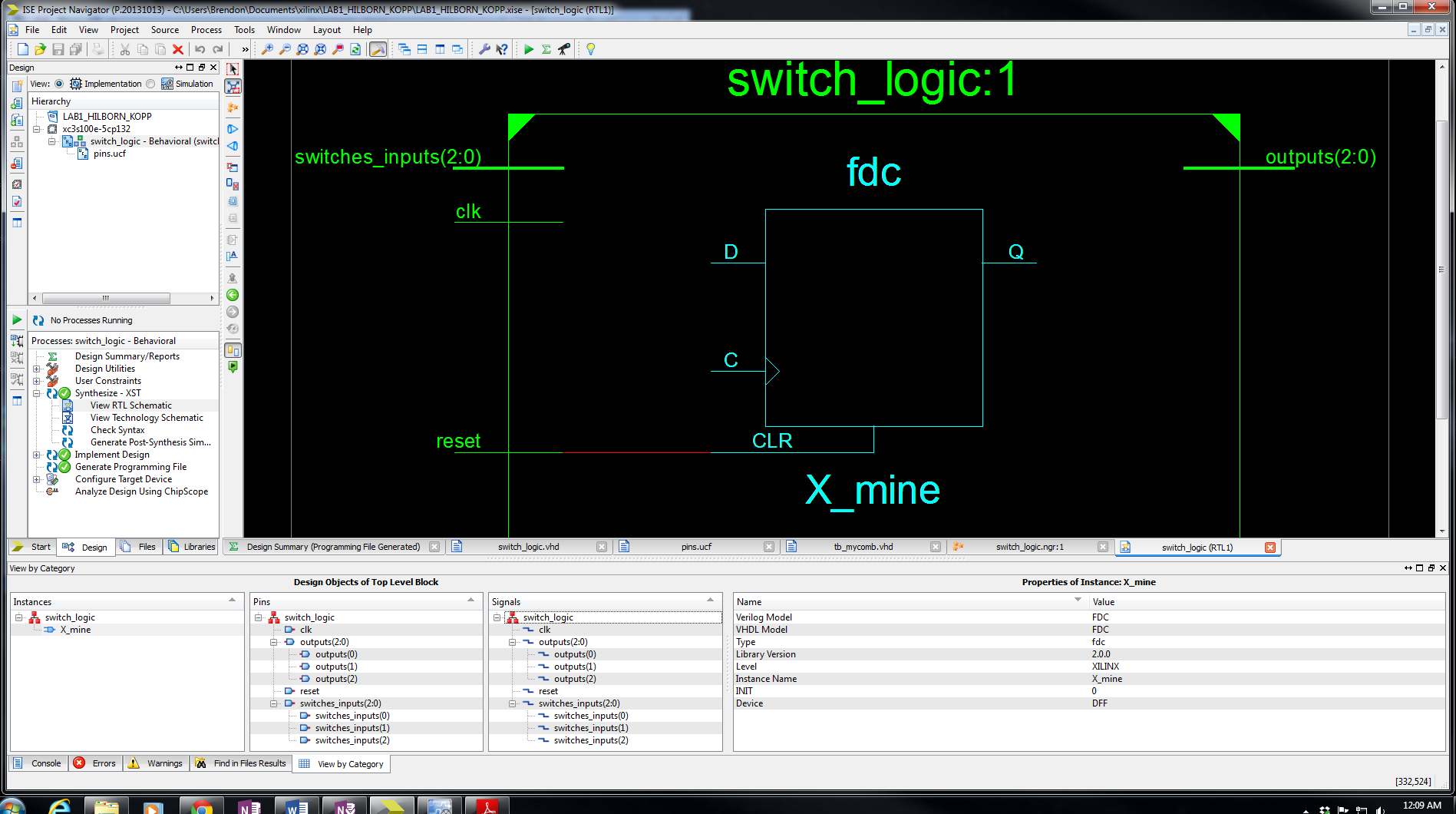
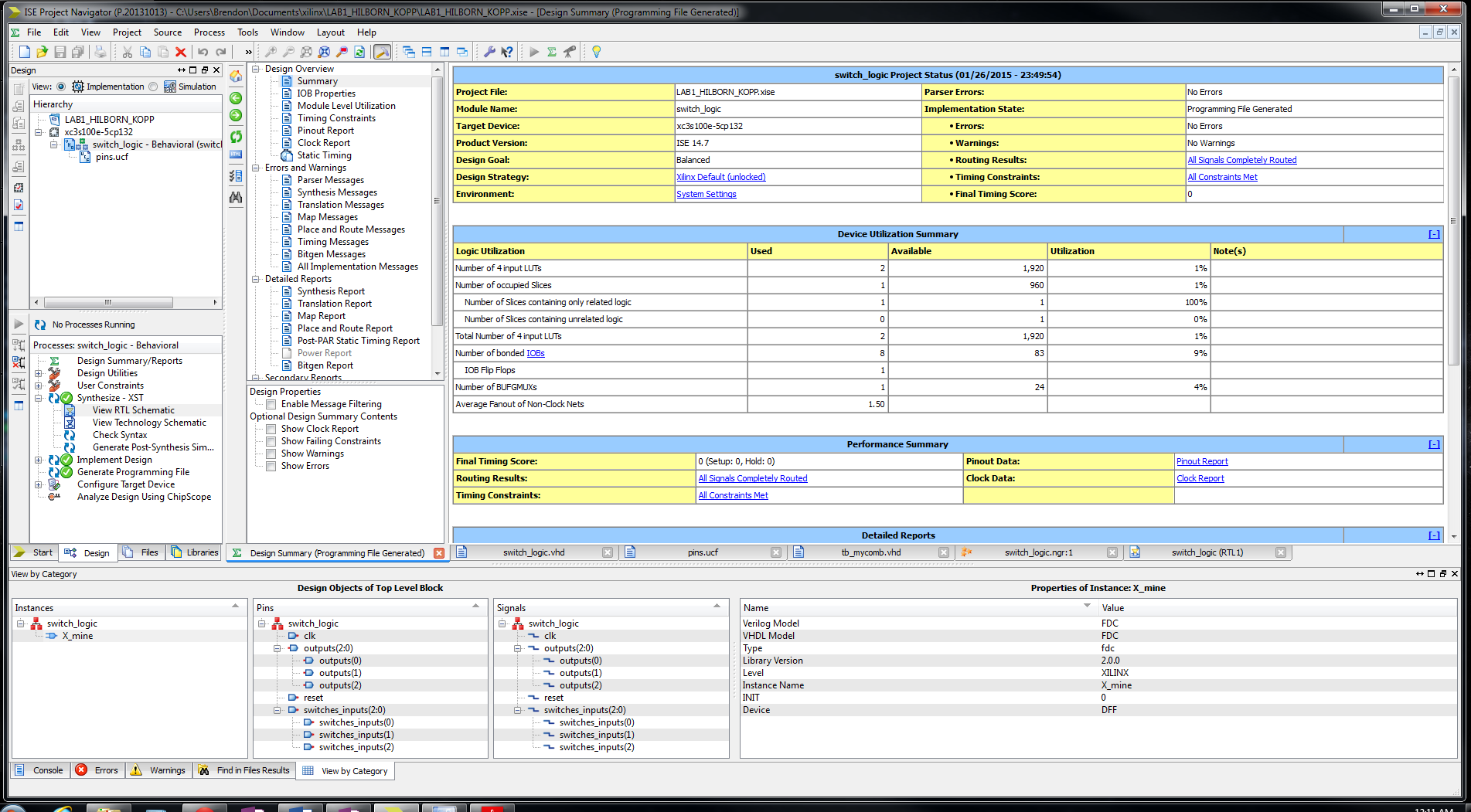
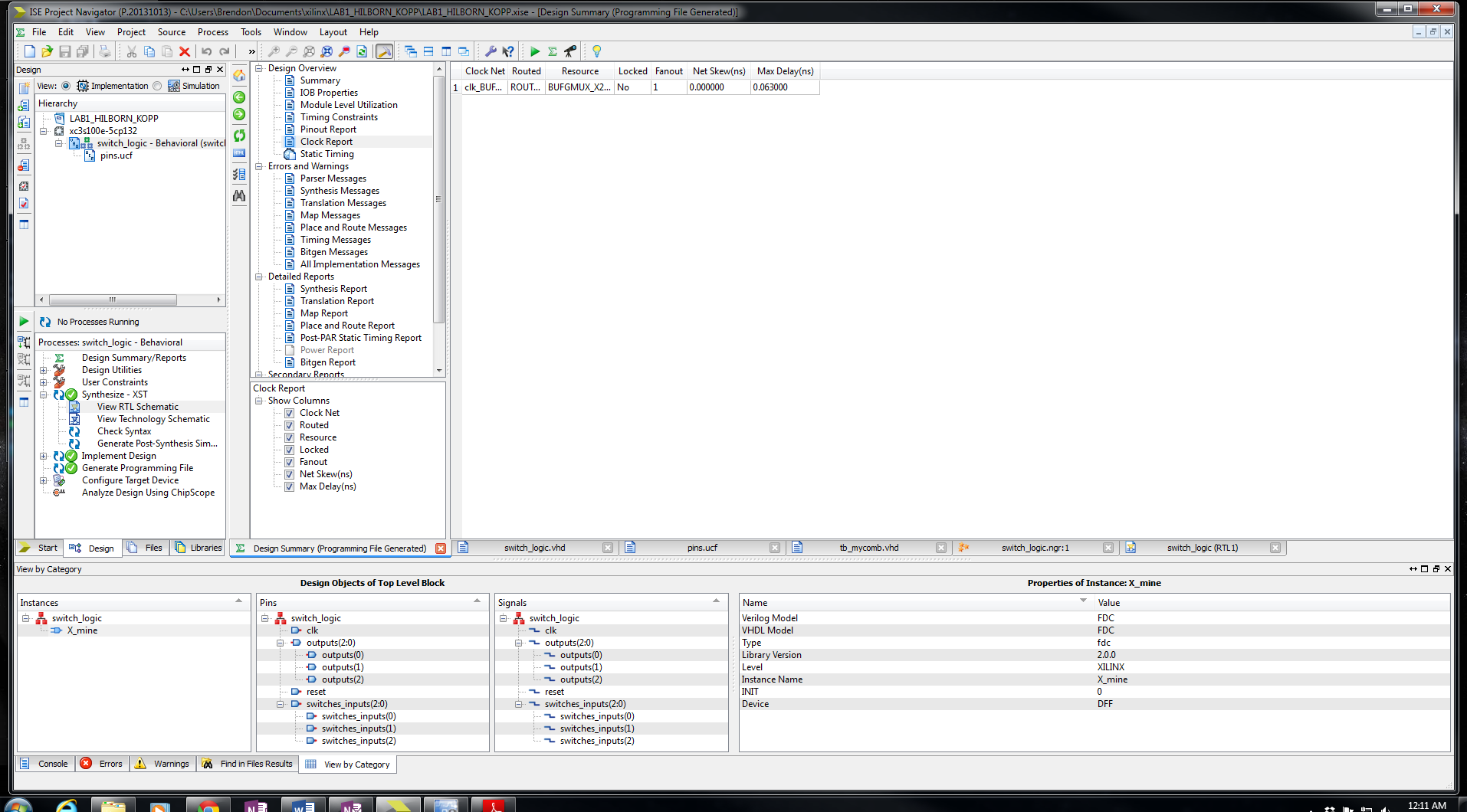
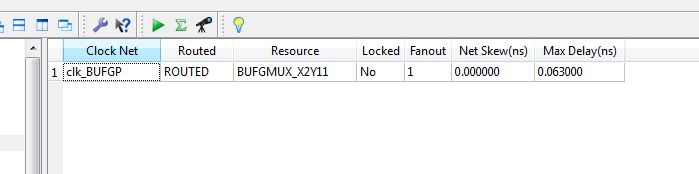
Screenshots:











**PAR static timing report:**

--------------------------------------------------------------------------------

Release 14.7 Trace (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 5

-n 3 -fastpaths -xml switch\_logic.twx switch\_logic.ncd -o switch\_logic.twr

switch\_logic.pcf -ucf pins.ucf

Design file: switch\_logic.ncd

Physical constraint file: switch\_logic.pcf

Device,package,speed: xc3s100e,cp132,-5 (PRODUCTION 1.27 2013-10-13)

Report level: verbose report

Environment Variable Effect

-------------------- ------

NONE No environment variables were set

--------------------------------------------------------------------------------

INFO:Timing:2698 - No timing constraints found, doing default enumeration.

INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).

INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths

option. All paths that are not constrained will be reported in the

unconstrained paths section(s) of the report.

INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on

a 50 Ohm transmission line loading model. For the details of this model,

and for more information on accounting for different loading conditions,

please see the device datasheet.

INFO:Timing:3390 - This architecture does not support a default System Jitter

value, please add SYSTEM\_JITTER constraint to the UCF to modify the Clock

Uncertainty calculation.

INFO:Timing:3389 - This architecture does not support 'Discrete Jitter' and

'Phase Error' calculations, these terms will be zero in the Clock

Uncertainty calculation. Please make appropriate modification to

SYSTEM\_JITTER to account for the unsupported Discrete Jitter and Phase

Error.

Data Sheet report:

-----------------

All values displayed in nanoseconds (ns)

Setup/Hold to clock clk

------------------+------------+------------+------------------+--------+

|Max Setup to|Max Hold to | | Clock |

Source | clk (edge) | clk (edge) |Internal Clock(s) | Phase |

------------------+------------+------------+------------------+--------+

switches\_inputs<0>| 2.852(R)| -1.102(R)|clk\_BUFGP | 0.000|

switches\_inputs<1>| 3.820(R)| -1.877(R)|clk\_BUFGP | 0.000|

switches\_inputs<2>| 3.427(R)| -1.562(R)|clk\_BUFGP | 0.000|

------------------+------------+------------+------------------+--------+

Clock clk to Pad

------------+------------+------------------+--------+

| clk (edge) | | Clock |

Destination | to PAD |Internal Clock(s) | Phase |

------------+------------+------------------+--------+

outputs<2> | 5.774(R)|clk\_BUFGP | 0.000|

------------+------------+------------------+--------+

Pad to Pad

------------------+---------------+---------+

Source Pad |Destination Pad| Delay |

------------------+---------------+---------+

switches\_inputs<0>|outputs<0> | 6.445|

switches\_inputs<0>|outputs<1> | 7.073|

switches\_inputs<1>|outputs<0> | 7.363|

switches\_inputs<1>|outputs<1> | 8.041|

switches\_inputs<2>|outputs<0> | 7.026|

switches\_inputs<2>|outputs<1> | 7.648|

------------------+---------------+---------+

Analysis completed Mon Jan 26 23:49:43 2015

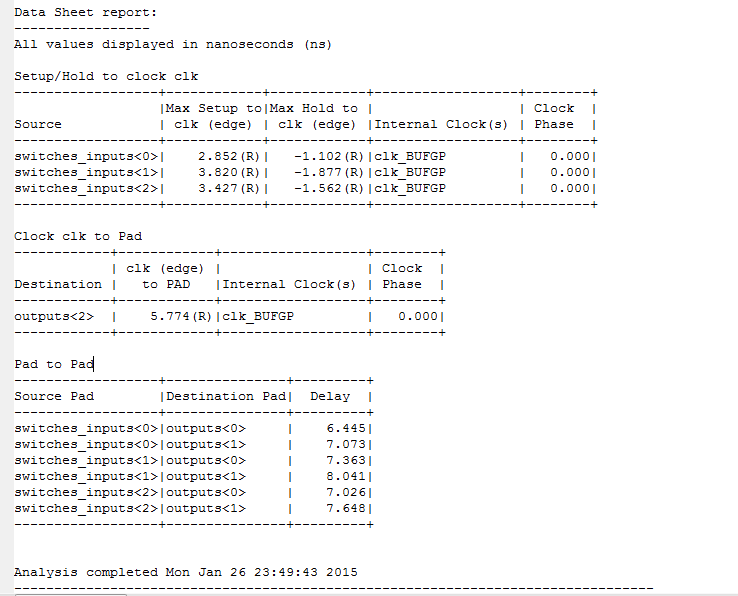
--------------------------------------------------------------------------------

Trace Settings:

-------------------------

Trace Settings

Peak Memory Usage: 150 MB



**Synthesis Report (has timing stuff):**

Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Reading design: switch\_logic.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Compilation

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "switch\_logic.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "switch\_logic"

Output Format : NGC

Target Device : xc3s100e-5-cp132

---- Source Options

Top Module Name : switch\_logic

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 24

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Users/Brendon/Documents/xilinx/LAB1\_HILBORN\_KOPP/switch\_logic.vhd" in Library work.

Architecture behavioral of Entity switch\_logic is up to date.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <switch\_logic> in library <work> (architecture <behavioral>).

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing Entity <switch\_logic> in library <work> (Architecture <behavioral>).

Entity <switch\_logic> analyzed. Unit <switch\_logic> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <switch\_logic>.

Related source file is "C:/Users/Brendon/Documents/xilinx/LAB1\_HILBORN\_KOPP/switch\_logic.vhd".

Found 1-bit register for signal <X\_mine>.

Summary:

inferred 1 D-type flip-flop(s).

Unit <switch\_logic> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Registers : 1

1-bit register : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Registers : 1

Flip-Flops : 1

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <switch\_logic> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block switch\_logic, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Macro Statistics

# Registers : 1

Flip-Flops : 1

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : switch\_logic.ngr

Top Level Output File Name : switch\_logic

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 8

Cell Usage :

# BELS : 2

# LUT3 : 2

# FlipFlops/Latches : 1

# FDC : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 7

# IBUF : 4

# OBUF : 3

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 3s100ecp132-5

Number of Slices: 1 out of 960 0%

Number of 4 input LUTs: 2 out of 1920 0%

Number of IOs: 8

Number of bonded IOBs: 8 out of 83 9%

IOB Flip Flops: 1

Number of GCLKs: 1 out of 24 4%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 1 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

-----------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

reset | IBUF | 1 |

-----------------------------------+------------------------+-------+

Timing Summary:

---------------

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: 2.518ns

Maximum output required time after clock: 4.040ns

Maximum combinational path delay: 5.799ns

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 3 / 1

-------------------------------------------------------------------------

Offset: 2.518ns (Levels of Logic = 2)

Source: switches\_inputs<1> (PAD)

Destination: X\_mine (FF)

Destination Clock: clk rising

Data Path: switches\_inputs<1> to X\_mine

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 2 1.106 0.532 switches\_inputs\_1\_IBUF (switches\_inputs\_1\_IBUF)

LUT3:I0->O 2 0.612 0.000 X\_th1 (outputs\_1\_OBUF)

FDC:D 0.268 X\_mine

----------------------------------------

Total 2.518ns (1.986ns logic, 0.532ns route)

(78.9% logic, 21.1% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 1 / 1

-------------------------------------------------------------------------

Offset: 4.040ns (Levels of Logic = 1)

Source: X\_mine (FF)

Destination: outputs<2> (PAD)

Source Clock: clk rising

Data Path: X\_mine to outputs<2>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 1 0.514 0.357 X\_mine (X\_mine)

OBUF:I->O 3.169 outputs\_2\_OBUF (outputs<2>)

----------------------------------------

Total 4.040ns (3.683ns logic, 0.357ns route)

(91.2% logic, 8.8% route)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 6 / 2

-------------------------------------------------------------------------

Delay: 5.799ns (Levels of Logic = 3)

Source: switches\_inputs<1> (PAD)

Destination: outputs<1> (PAD)

Data Path: switches\_inputs<1> to outputs<1>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 2 1.106 0.532 switches\_inputs\_1\_IBUF (switches\_inputs\_1\_IBUF)

LUT3:I0->O 2 0.612 0.380 X\_th1 (outputs\_1\_OBUF)

OBUF:I->O 3.169 outputs\_1\_OBUF (outputs<1>)

----------------------------------------

Total 5.799ns (4.887ns logic, 0.912ns route)

(84.3% logic, 15.7% route)

=========================================================================

Total REAL time to Xst completion: 3.00 secs

Total CPU time to Xst completion: 3.09 secs

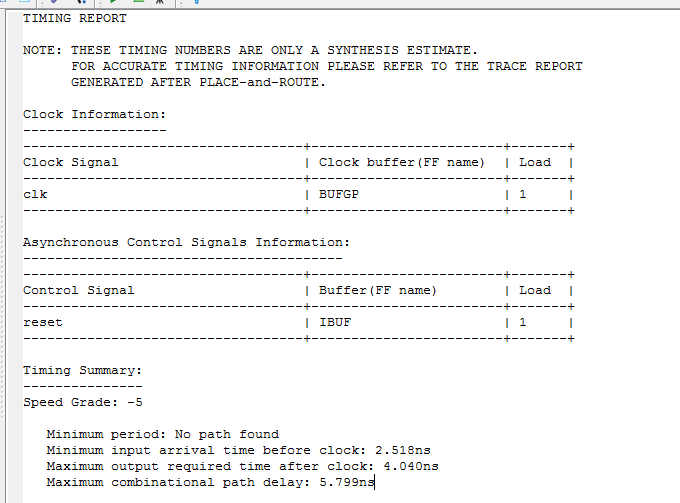
-->

Total memory usage is 256168 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)



**Place and route report:**

Release 14.7 par P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

BRENDON-PC:: Mon Jan 26 23:49:37 2015

par -w -intstyle ise -ol high -t 1 switch\_logic\_map.ncd switch\_logic.ncd

switch\_logic.pcf

Constraints file: switch\_logic.pcf.

Loading device for application Rf\_Device from file '3s100e.nph' in environment C:\Xilinx\14.7\ISE\_DS\ISE\.

"switch\_logic" is an NCD, version 3.2, device xc3s100e, package cp132, speed -5

Initializing temperature to 85.000 Celsius. (default - Range: -40.000 to 100.000 Celsius)

Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.320 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par

-x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all

internal clocks in this design. Because there are not defined timing requirements, a timing score will not be

reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.

Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.27 2013-10-13".

Design Summary Report:

Number of External IOBs 8 out of 83 9%

Number of External Input IOBs 5

Number of External Input IBUFs 5

Number of LOCed External Input IBUFs 5 out of 5 100%

Number of External Output IOBs 3

Number of External Output IOBs 3

Number of LOCed External Output IOBs 3 out of 3 100%

Number of External Bidir IOBs 0

Number of BUFGMUXs 1 out of 24 4%

Number of Slices 1 out of 960 1%

Number of SLICEMs 0 out of 480 0%

Overall effort level (-ol): High

Placer effort level (-pl): High

Placer cost table entry (-t): 1

Router effort level (-rl): High

Starting initial Timing Analysis. REAL time: 1 secs

Finished initial Timing Analysis. REAL time: 1 secs

Starting Placer

Total REAL time at the beginning of Placer: 1 secs

Total CPU time at the beginning of Placer: 0 secs

Phase 1.1 Initial Placement Analysis

Phase 1.1 Initial Placement Analysis (Checksum:17d0aac) REAL time: 2 secs

Phase 2.7 Design Feasibility Check

Phase 2.7 Design Feasibility Check (Checksum:17d0aac) REAL time: 2 secs

Phase 3.31 Local Placement Optimization

Phase 3.31 Local Placement Optimization (Checksum:17d0aac) REAL time: 2 secs

Phase 4.2 Initial Clock and IO Placement

Phase 4.2 Initial Clock and IO Placement (Checksum:1d8ccec) REAL time: 2 secs

Phase 5.30 Global Clock Region Assignment

Phase 5.30 Global Clock Region Assignment (Checksum:1d8ccec) REAL time: 2 secs

Phase 6.36 Local Placement Optimization

Phase 6.36 Local Placement Optimization (Checksum:1d8ccec) REAL time: 2 secs

Phase 7.8 Global Placement

.....

Phase 7.8 Global Placement (Checksum:2219523) REAL time: 2 secs

Phase 8.5 Local Placement Optimization

Phase 8.5 Local Placement Optimization (Checksum:2219523) REAL time: 2 secs

Phase 9.18 Placement Optimization

Phase 9.18 Placement Optimization (Checksum:2376807) REAL time: 2 secs

Phase 10.5 Local Placement Optimization

Phase 10.5 Local Placement Optimization (Checksum:2376807) REAL time: 2 secs

Total REAL time to Placer completion: 2 secs

Total CPU time to Placer completion: 1 secs

Writing design to file switch\_logic.ncd

Starting Router

Phase 1 : 13 unrouted; REAL time: 3 secs

Phase 2 : 11 unrouted; REAL time: 3 secs

Phase 3 : 2 unrouted; REAL time: 3 secs

Phase 4 : 2 unrouted; (Par is working to improve performance) REAL time: 3 secs

Phase 5 : 0 unrouted; (Par is working to improve performance) REAL time: 3 secs

Updating file: switch\_logic.ncd with current fully routed design.

Phase 6 : 0 unrouted; (Par is working to improve performance) REAL time: 3 secs

Phase 7 : 0 unrouted; (Par is working to improve performance) REAL time: 3 secs

Phase 8 : 0 unrouted; (Par is working to improve performance) REAL time: 3 secs

Phase 9 : 0 unrouted; (Par is working to improve performance) REAL time: 3 secs

Total REAL time to Router completion: 3 secs

Total CPU time to Router completion: 1 secs

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

Generating "PAR" statistics.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Generating Clock Report

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

+---------------------+--------------+------+------+------------+-------------+

| Clock Net | Resource |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|

+---------------------+--------------+------+------+------------+-------------+

| clk\_BUFGP | BUFGMUX\_X2Y11| No | 1 | 0.000 | 0.063 |

+---------------------+--------------+------+------+------------+-------------+

\* Net Skew is the difference between the minimum and maximum routing

only delays for the net. Note this is different from Clock Skew which

is reported in TRCE timing report. Clock Skew is the difference between

the minimum and maximum path delays which includes logic delays.

\* The fanout is the number of component pins not the individual BEL loads,

for example SLICE loads not FF loads.

Timing Score: 0 (Setup: 0, Hold: 0)

Asterisk (\*) preceding a constraint indicates it was not met.

This may be due to a setup or hold violation.

------------------------------------------------------------------------------------------------------

Constraint | Requested | Actual | Logic | Absolute |Number of

| | | Levels | Slack |errors

------------------------------------------------------------------------------------------------------

All constraints were met.

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 3 secs

Total CPU time to PAR completion: 1 secs

Peak Memory Usage: 321 MB

Placement: Completed - No errors found.

Routing: Completed - No errors found.

Number of error messages: 0

Number of warning messages: 0

Number of info messages: 1

Writing design to file switch\_logic.ncd

PAR done!

